IN THE SPECIFICATION:

Please amend the paragraph beginning on page 13, line 14 as follows:

The slice 302 receives signals from an address generator 326 via signal path S11 and a memory interface 328 via signal path S12. Specifically, the address MUX 310 receives a stream identifier from the address generator 326 and an address signal from the memory interface 328. The address generator 326 operates as a controller that produces the appropriate phase and phase increment values to the adder 304 to facilitate mulitple ~~frequcy cock~~frequency clock generation. In this case, the stream identifier may comprise an 8-bit binary symbol identifying one of the 256 users. The address signal identifies the location of data within a dual port memory that is a phase accumulator value that represents the accumulated phase for an oscillator producing a clock signal for that user's data. The address signal also identifies the memory location of a phase increment value within the phase increment value storage 308. The phase accumulator value storage 306 represents 64 virtual phase accumulators and the phase increment value storage 308 represents 64 virtual phase increment registers. These individual virtual phase accumulators and virtual phase increment registers are physically implemented using timely recall of the accumulator and increment values from a dual port memory within a field programmable gate array (FPGA).